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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/649,746 | 08/28/2003 | Fukashi Harada | 031071 | 5719 |
| 23850 | 7590 | 10/12/2004 | EXAMINER | |
| ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP 1725 K STREET, NW SUITE 1000 WASHINGTON, DC 20006 | | | NADAV, ORI | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2811 | |

DATE MAILED: 10/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | | |
|------------------------------|-------------------------------|-------------------------------|--|
| Office Action Summary | Application No. 10/649,746 | Applicant(s) HARADA ET AL. | |
| | Examiner ori nadav | Art Unit 2811 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 03 September 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 4, 6, 8, 9, 11, 12, 14, 16, 17, 19, 20 and 22 is/are rejected.
- 7) ☒ Claim(s) 3, 5, 7, 10, 13, 15, 18 and 21 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 August 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

Figure 8 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: The recitation of a "circle in figure 5/6" (see pages 11 and 13) is not illustrated in figures 5 and 6.

The disclosure should describe forming a compound semiconductor film which contains silicon and another semiconductor element, and has a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the other semiconductor element in an intermediate layer region, as recited in claims 1 and 8.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-2, 4, 6, 8-9, 11-12, 14, 16-17, 19-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Asai et al. (6,713,790) in view of Applicant Admitted Prior Art (AAPA).

Regarding claims 1, 8 and 11, Asai et al. teach in figures 7-11 a manufacturing method of a semiconductor device which is formed with a bipolar transistor being composed by including a base, an emitter and a collector on a semiconductor substrate, comprising the steps of:

forming a multilayer film 115, 117, 120 on said semiconductor substrate 100, and forming an opening which is opened on said base and said emitter, in the multilayer film;

forming on an entire surface a compound semiconductor film 111 which contains silicon and another semiconductor element; and

performing anisotropic dry etching (column 20, lines 19-27) for the compound semiconductor film so as to reach a certain height of the opening, but performing no isotropic etching.

Note that the broad recitation of the claim does not require the compound semiconductor film to be anisotropic dry etched, because anisotropic dry etching

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is performed for the compound semiconductor film, in contrast to anisotropic dry etching the compound semiconductor film.

Asai et al. do not teach a compound semiconductor film having a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the other semiconductor element in an intermediate layer region.

AAPA teaches in pages 2-3 that it is conventional to obtain a compound semiconductor film which contains silicon and another semiconductor element, and has a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the other semiconductor element in an intermediate layer region

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a compound semiconductor film having a composition with a high content of silicon in an upper layer region and a lower layer region, and a high content of the other semiconductor element in an intermediate layer region in Asai et al.'s device in order to simplify the processing steps of making the device by using a conventional processing method.

Regarding claims 2 and 9, Asai et al. teach using a high vacuum (column 3, lines 56-57). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an anisotropic dry etching in a high vacuum in Asai et al.'s device in order to obtain better etching performance.

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Regarding claims 4, 6, 12 and 14, Asai et al. do not teach the atmospheric pressure in the high vacuum state is lower than 66.5 Pa and about 0.33 Pa. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use an atmospheric pressure in the high vacuum state of Asai et al.'s device to be lower than 66.5 Pa and about 0.33 Pa in order to obtain proper etching conditions.

Regarding claims 16-17, 19-20 and 22, Asai et al. teach the compound semiconductor film comprises an SiGe film or an SiGeC film.

Response to Arguments

Applicant argues that figure 8 is not a prior art, because the specification merely recites on page 3, lines 3 et seq., "the semiconductor film . . . which is used here", meaning the semiconductor film as used in the present invention.

The semiconductor film recited on page 3, line 3 refers to the semiconductor film recited in the conventional example of manufacturing, which was described in previous paragraph. The phrase "the semiconductor film . . . which is used here", refers to the semiconductor film which is used in the conventional example of manufacturing. Therefore, figure 8 should be labeled as "prior art".

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Applicant argues that an artisan would not be motivated to combine the semiconductor compound of AAPA with Asai et al., because the semiconductor compound of AAPA comprises voids.

AAPA's device prevents leakage current and impurity diffusion. Voids are introduced in the semiconductor compound of AAPA when isotropic plasma etching is used. However, Asai et al.'s device is not formed by using isotropic plasma etching. Therefore, an artisan would be motivated to combine the semiconductor compound of AAPA with Asai et al.

Allowable Subject Matter

Claims 3, 5, 7, 10, 13, 15, 18 and 21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Reasons for allowance

The following is an examiner's statement of reasons for allowance: . Asai et al. (6,713,790) and Applicant Admitted Prior Art (AAPA) teach substantially the entire claimed structure, as recited in claims 1 and 18, except the specific processing steps which are recited in claims 3, 5, 7, 10, 13, 15, 18 and 21. Therefore, prior art do not teach or render obviousness the semiconductor structure, as claimed.

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Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308- 0956**



O.N.
10/7/04

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800